CURRENT STEERING DIGITAL-TO-ANALOG (DAC) CONVERTER WITH IMPROVED DYNAMIC PERFORMANCE

FIELD OF THE INVENTION

[0001] This invention relates generally to digital-to-analog converters (DACs), and in particular, to a current steering DAC including a control circuit to improve its dynamic performance and output signal quality.

BACKGROUND OF THE INVENTION

[0002] Figure 1 illustrates a schematic diagram of a typical current steering digital-to-analog converter (DAC) 100. The current steering DAC 100 consists of a plurality of segments 110-1 to 110-n for selectively steering current to either the positive output OUTP or the negative output OUTN. Each of the current steering segments, as represented by segment 110n, consists of a current-setting field effect transistor (FET) M1n, a cascode FET M2n, and a pair of differential FETs M3n and M4n.

[0003] The current steering DAC 100 may further consists of a thermometer code decoder 120 including a switch driver 122 which receives the binary coded digital input signal that is to be converted into a differential analog signal at the outputs OUTP and OUTN of the current steering DAC 100 and generates the appropriate driving signals D1 to Dn and DB1 to DBn, in response to a conversion clock signal, for respectively controlling the current steering of the current steering segments 110-1 to 110-n. For instance, as the value of the input digital signal increases, the thermometer code decoder 120 generates binary signals D1 to Dn and DB1 to DBn to cause more current steering segments 110-1 to 110n to steer current to the positive output of the DAC 100. Conversely, as the value of the input digital signal decreases, the thermometer code decoder 120 generates binary signals D1 to Dn and DB1 to DBn to cause less current steering segments 110-1 to 110n to steer current to the positive output of the DAC 100.

[0004] More specifically, the source of each of the current-setting FETs M1n is connected to a power supply terminal AVDD, the gate of each of the current-setting FETs M1n receives a control voltage V_{GATE}, and the drain of each of the current-setting FETs M1n is connected to the source of the corresponding cascode FET M2n. The gate of each of the cascode FETs M2n receives a control voltage V_{CASC}, and the drain of each of the cascode FETs M2n is connected to the corresponding sources of the differential FET pair M3n and M4n. The gates of each of the differential FET pair M3n and M4n respectively receive the corresponding control signals Dn and DBn generated by the thermometer code decoder 120. The drains of each of the differential FET pair M3n and M4n are coupled respectively to the positive output OUTP and negative output OUTN of the current steering DAC 100.

[0005] The control voltage V_{GATE} sets the current through each of the current steering segments 110-1 to 110-n. The control voltage V_{CASC} sets the drain-to-source voltage of the current-setting FETs M11 to M1n in a manner that the output impedances of the current steering segments 110-1 to 110-n are relatively high. The control signals Dn and DBn causes the corresponding differential FET pairs M3n and M4n to steer the current to either the positive output OUTP or the negative output OUTN. For example, if the control signal Dn is a logic high and DBn is a logic low, differential FET M3n is turned "off" and differential FET M4n is turned "on". Accordingly, the current in the corresponding current steering segment 110n is steered to the negative output OUTN of the DAC 100. Conversely, if the control signal Dn is a logic low and DBn is a logic high, differential FET M3n is turned "on" and differential FET M4n is turned "off". Accordingly, the current in the corresponding current steering segment 110n is steered to the positive output OUTP of the DAC 100.

[0006] A drawback of the current steering DAC 100 stems from the fact that as a current steering segment 110n changes the current steering between the positive and negative outputs OUTP and OUTN (which are typically at different voltage levels), the voltage at the summing node Sn (at the sources of the differential FET pair M3n and M4n) shifts due to the finite intrinsic gain of

the differential FET pair M3n and M4n. The shifting of the voltage at the summing node Sn is proportional to the voltage difference between the voltages on the positive and negative outputs OUTP and OUTN of the DAC 100. When this voltage shifts, the capacitance at the summing node Sn has to be recharged. The charge flowing to the capacitance affects the converter output signal, and creates harmonic distortion. This distortion is more prevalent at higher output tone frequency. Thus, the dynamic range of the DAC 100, typically referred to in the art as the Spurious Free Dynamic Range (SFDR), is limited by the shifting voltage at the summing node Sn.

[0007] Accordingly, there is a need for an apparatus and method which reduces the variation of the voltage at each of the summing nodes to improve the dynamic range and output signal quality of the DAC. Such need and other are addressed in the detailed description of the invention as follows.

SUMMARY OF THE INVENTION

[0008] An aspect of the invention relates to a current steering digital-to-analog (DAC) having improved dynamic performance and output signal quality. The current steering DAC comprises a plurality of current steering segments each including differential transistors to steer a current from a summing node to either a positive output or negative output of the DAC. The current steering DAC further comprises a control circuit to reduce a variation of a voltage present at the summing node of each of the current steering segments. By reducing the variation in the summing node voltages, improved dynamic performance and output signal quality can be achieved.

[0009] More specifically, the control circuit comprises a first control circuit to reduce the variation of the voltage present at the summing node of each of the current steering segments that are currently steering current to the positive output in response to the voltage present at the positive output of the DAC. In addition, the control circuit comprises a second control circuit to reduce the variation of the voltage present at the summing node of each of the current

steering segments that are currently steering current to the negative output in response to the voltage present at the negative output of the DAC.

[00010] The first control circuit may comprise an operational amplifier including positive and negative input terminals and an output terminal, wherein the output terminal is coupled to the substrate (i.e. bulk) terminals of the differential transistors that are electrically connected to the positive output; a reference voltage source coupled to the positive input terminal of the operational amplifier; and a field effect transistor (FET) including a source electrically connected to the negative input terminal of the operational amplifier, a drain electrically connected to the positive output of the DAC, a gate electrically connected to ground, and a substrate (i.e. bulk) terminal electrically connected to the output terminal of the operational amplifier. The operational amplifier generates a voltage that controls the threshold voltages of the differential transistors that are electrically connected to the positive output of the DAC in a manner that the voltages at the respective summing nodes of the current steering segments currently steering currents to the positive output of the DAC are substantially constant.

[00011] The second control circuit may comprise an operational amplifier including positive and negative input terminals and an output terminal, wherein the output terminal is coupled to the substrate (i.e. bulk) terminals of the differential transistors that are electrically connected to the negative output of the DAC; a reference voltage source coupled to the positive input terminal of the operational amplifier; and a FET including a source electrically connected to the negative input terminal of the operational amplifier, a drain electrically connected to the negative output of the DAC, a gate electrically connected to ground, and a substrate (i.e. bulk) terminal electrically connected to the output terminal of the operational amplifier. The operational amplifier generates a voltage that controls the threshold voltages of the differential transistors that are electrically connected to the negative output of the DAC in a manner that the voltages at the respective summing nodes of the current steering segments

currently steering currents to the negative output of the DAC are substantially constant.

[00012] To maintain the summing node voltages substantially constant in a preferred way, the FETs of the current steering segments are sized and laid out such that they comprise fingers of the same length and width as the FETs of the first and second control circuits. In addition, the drain currents of the control circuit FETs are set such that their current per finger is substantially the same as in the current steering segments' FETs.

[00013] Another aspect relates to a method of converting an input digital signal to a differential analog output signal. The method comprises steering currents from respective summing nodes to positive and/or negative outputs of a DAC in response to the input digital signal to generate a differential analog output signal; and reducing the variations of the voltages present respectively at the summing nodes. Again, by reducing the variation in the summing node voltages, improved dynamic performance and output signal quality can be achieved.

[00014] The reducing of the variation of the summing node voltages may comprise sensing a variation of the voltage at the positive output; and reducing the variations of the voltages at a portion of the summing nodes in response to the variation of the voltage at the positive output. More specifically, this may entail comparing the voltage at the positive output with a substantially constant voltage; and reducing the variations of the voltages at the portion of the summing nodes in response to an outcome of the comparison. This may further entail providing differential transistors to steer the currents from respective summing nodes to the positive output, and controlling the threshold voltages of the differential transistors electrically connected to the positive output.

[00015] Similarly, the reducing of the variations of the summing node voltages may comprise sensing a variation of the voltage at the negative output; and reducing the variations of the voltage at a portion of the summing nodes in response to the variation of the voltage at the negative output. More specifically, this may entail comparing the voltage at the negative output with a

substantially constant voltage; and reducing the variations of the voltages at a portion of the summing nodes in response to an outcome of the comparison. This may further entail providing differential transistors to steer the currents from respective summing nodes to the negative output, and controlling the threshold voltages of the differential transistors electrically connected to the negative output.

[00016] Other aspects, features, and techniques of the invention will be apparent to one skilled in the relevant art in view of the following detailed description of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[00017] Figure 1 illustrates a schematic diagram of a typical current steering digital-to-analog converter (DAC); and

[00018] Figure 2 illustrates a schematic diagram of an exemplary current steering digital-to-analog converter (DAC) in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[00019] Figure 2 illustrates a schematic diagram of an exemplary current steering digital-to-analog converter (DAC) 200 in accordance with an embodiment of the invention. The current steering DAC 200 comprises a plurality of segments 210-1 to 210-n for selectively steering current to either the positive output OUTP or the negative output OUTN, respectively. Each of the current steering segments, as represented by segment 210n, comprises a current-setting field effect transistor (FET) M1n, a cascode FET M2n, and a pair of differential FETs M3n and M4n.

[00020] The current steering DAC 200 may further comprise a thermometer code decoder 220 including a switch driver 222 which receives the binary coded digital input signal that is to be converted into a differential analog signal at the outputs OUTP and OUTN of the current steering DAC 200 and generates the appropriate driving signals D1 to Dn and DB1 to DBn, in response to a

conversion clock signal, for respectively controlling the current steering of the current steering segments 210-1 to 210-n.

[00021] The source of each of the current-setting FETs M1n is connected to a power supply terminal AVDD, the gate of each of the current-setting FETs M1n receives a control voltage V_{GATE}, and the drain of each of the current-setting FETs M1n is connected to the source of the corresponding cascode FET M2n. The gate of each of the cascode FETs M2n receives a control voltage V_{CASC}, and the drain of each of the cascode FETs M2n is connected to the corresponding sources of the differential FET pair M3n and M4n. The gates of each of the differential FET pair M3n and M4n respectively receive the corresponding control signals Dn and DBn generated by the thermometer code decoder 220. The drains of each of the differential FET pair M3n and M4n are coupled respectively to the positive output OUTP and negative output OUTN of the current steering DAC 200.

[00022] The control voltage V_{GATE} sets the current through each of the current steering segments 210-1 to 210-n. The control voltage V_{CASC} sets the drain-to-source voltage of the current-setting FETs M11 to M1n in a manner that the output impedances of the current steering segments 210-1 to 210-n are relatively high. The control signals Dn and DBn causes the corresponding differential FET pairs M3n and M4n to steer the current to either the positive output OUTP or the negative output OUTN.

[00023] As discussed in the Background Section, the variations of the voltages present at the summing nodes Sn as the corresponding differential FET pairs M3n and M4n are switched, have adverse effects on the dynamic range and signal quality of the output of the current steering DAC. In other words, such variation degrade or limit the SFDR characteristic of a DAC. To alleviate this problem, the current steering DAC 200 in accordance with the invention further includes a control circuit to reduce the variation of the voltages at the summing nodes Sn, thereby improving the dynamic performance and signal quality of the output of the current steering DAC 200.

[00024] In particular, the current steering DAC 200 further comprises a first control circuit 230P responsive to the voltage at the positive output OUTP to control the threshold voltages of FETs M31 to M3n (the transistors connected to the positive output OUTP) such that the variations of the voltages at the summing nodes Sn are substantially reduced. Similarly, the current steering DAC 200 further comprises a second control circuit 230N responsive to the voltage at the negative output OUTN to control the threshold voltages of FETs M41 to M4n such that the variations of the voltages at the summing nodes Sn are substantially reduced.

[00025] More specifically, the first control circuit 230P comprises an operational amplifier 240P and FETs M5P and M6P. FET M5P includes a source electrically connected to the positive input terminal of the operational amplifier 240P and to the power supply terminal AVDD by way of a current source 242P, and a gate and drain electrically connected to a ground terminal. FET M6P includes a source electrically connected to the negative input terminal of the operational amplifier 240P and to the power supply terminal AVDD by way of a current source 244P (a resistor, FET or other device), a gate electrically connected to the ground terminal, and a drain electrically connected to the positive output OUTP of the current steering DAC 200. The FET6P further includes a substrate terminal (i.e. bulk terminal) electrically connected to the output of the operational amplifier 240P.

[00026] Similarly, the second control circuit 230N comprises an operational amplifier 240N and FETs M5N and M6N. FET M5N includes a source electrically connected to the positive input terminal of the operational amplifier 240N and to the power supply terminal AVDD by way of a current source 244N (a resistor, FET or other device), and a gate and drain electrically connected to the ground terminal. FET M6N includes a source electrically connected to the negative input terminal of the operational amplifier 240N and to the power supply terminal AVDD by way of a current source 242N, a gate electrically connected to the ground terminal, and a drain electrically connected to the negative output OUTN of the current steering DAC 200. The FET6N further

includes a substrate terminal (i.e. bulk terminal) electrically connected to the output of the operational amplifier 240N.

[00027] The operation of the first control circuit 230P is discussed as follows. FET M5P is diode-connected between the power supply terminal AVDD by way of the current source 242P, and ground terminal, thereby providing a substantially constant reference voltage to the positive input of the operational amplifier 240P. The voltage at the source of FET M6P, which is susceptible to variation due to variation of the voltage at the positive output OUTP of the current steering DAC 200, is applied to the negative input terminal of the operational amplifier 240P, and thereby provides negative feedback for the control operation. The operational amplifier 240P produces a voltage that controls the threshold voltage of the FET M6P in a manner that the source voltage of FET M6P is substantially constant. In other words, the control of the threshold voltage changes the gate-to-source voltage relationship of the FET M6P such that its source voltage remains substantially constant. The output of the operational amplifier 240P is also coupled to the substrates (i.e. bulk) of FETs M31 to M3n, thereby also controlling their threshold voltages in a similar manner, i.e. such that their source voltages (i.e. the voltages at the summing nodes Sn) are maintained substantially constant.

[00028] To maintain the source voltages of FETs M31 to M3n substantially constant in a preferred way, the FETs M31 to M3n are sized and laid out such that they comprise fingers of substantially the same length and width as FET M6P. The drain current of FET M6P is set such that the current per finger in FET M6P is substantially the same as in FETs M31 to M3n. For preferred circuit operation, FET M5P has substantially the same size and drain current as FET M6P.

[00029] Similarly for the second control circuit 230N, FET M5N is diode-connected between the power supply terminal AVDD by way of the current source 244N, and ground terminal, thereby providing a substantially constant reference voltage to the positive input of the operational amplifier 240N. The voltage at the source of FET M6N, which is susceptible to variation due to

variation of the voltage at the negative output OUTN of the current steering DAC 200, is applied to the negative input terminal of the operational amplifier, and thereby provides negative feedback for the control operation. The operational amplifier 240N produces a voltage that controls the threshold voltage of the FET M6N in a manner that the source voltage of FET M6N is substantially constant. In other words, the control of the threshold voltage changes the gate-to-source voltage relationship of the FET M6N such that its source voltage remains substantially constant. The output of the operational amplifier 240N is also coupled to the substrates (i.e. bulk) of FETs M41 to M4n, thereby also controlling their threshold voltages in a similar manner, i.e. such that their source voltages (i.e. the voltages at the summing nodes Sn) are maintained substantially constant.

[00030] To maintain the source voltages of FETs M41 to M4n substantially constant in a preferred way, the FETs M41 to M4n are sized and laid out such that they comprise fingers of substantially the same length and width as FET M6N. The drain current of FET M6N is set such that the current per finger in FET M6N is substantially the same as in FETs M41 to M4n. For preferred circuit operation, FET M5N has the substantially same size and drain current as FET M6N.

[00031] The reduction in the variation of the voltages at the respective summing nodes Sn improves the dynamic performance and signal quality of the output of the current steering DAC 200 (i.e. improves the SFDR characteristic of the DAC 200). Thus, the current steering DAC 200 in accordance with the invention can be made to operate at higher frequencies and at the same time produce a differential output voltage with improved signal quality.

[00032] Although the exemplary embodiment of the current steering DAC 200 illustrated includes p-type FETs, it shall be understood that n-type FETs can also be used in place thereof. In addition, the current steering DAC 200 need not be limited to FET technology, but other transistor technologies can also be used, such as bipolar technology. Furthermore, a particular implementation of the first and second control circuit is illustrated, it shall be understood that other

implementations for reducing the variations of the voltages at the summing nodes are within the scope of the invention.

[00033] While the invention has been described in connection with various embodiments, it will be understood that the invention is capable of further modifications. This application is intended to cover any variations, uses or adaptation of the invention following, in general, the principles of the invention, and including such departures from the present disclosure as come within the known and customary practice within the art to which the invention pertains.